APPENDIX

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CLAIMS OF THE PARENT CASE (AS ALLOWED)

2. Multimedia interface, according to claim 3, wherein:
the reconfigurable logic is a field programmable gate array (FPGA).

3. Multimedia interface, comprising:
an integrated circuit (IC) chip;
a block of reconfigurable logic incorporated on the IC chip; and
a multimedia processor block incorporated on the IC chip separately from the reconfigurable logic;
further comprising at least one functional block selected from the group consisting of:
audio and/or video CODECs for interfacing to external analog multimedia signals;
phase locked loop (PLL) circuitry to reduce skew within various blocks within the IC chip and to synchronize to off-chip clock circuitry;
a programmable, fast serial interface core;
a programmable CPU interface core;
a programmable memory interface (PMI) core; and
power-down circuitry, in combination with one or more of these additional cores.

4. Multimedia interface, according to claim 3, wherein:
the multimedia processor block is implemented with 20k-40k gates; and
the reconfigurable logic block is implemented with at least 60k gates.

5. Multimedia interface, according to claim 3,
wherein:
the at least one functional block is the CODECs; and
the CODECs is implemented with approximately 10k gates.

6. Multimedia interface, according to claim 3, wherein:
the multimedia processor block is implemented with a first number (P) of gates; and
the reconfigurable logic block is implemented with a second number (L) of gates;
wherein:
the second number (L) is at least three times greater than the first number (P).

7. Multimedia interface, according to claim 6, wherein:
the at least one functional block is the CODECs; and
the CODECs is implemented with a third number (C) of gates; and
the second number (L) is at least six times greater than the third number (C).

8. Multimedia interface, according to claim 6, wherein:
the at least one functional block is the CODECs; and
the CODECs is implemented with a third number (C) of gates; and
the first number (P) is 2-4 times greater than the third number (C).

9. Multimedia interface, according to claim 3, wherein:
the multimedia processor block is implemented with a first number (P) of gates; and
the reconfigurable logic block is implemented with a second number (L) of gates; wherein:
the second number (L) is at least four times greater than the first number (P).

10. Multimedia interface, according to claim 9, wherein:
the at least one functional block is the CODECs; and
the CODECs is implemented with a third number (C) of gates; and
the second number (L) is at least six times greater than the third number (C).

11. Multimedia interface, according to claim 9, wherein:
the at least one functional block is the CODECs; and
the CODECs is implemented with a third number (C) of gates; and
the first number (P) is 2-4 times greater than the third number (C).

12. Multimedia interface, according to claim 3, wherein:
the multimedia processor block is implemented with a first number (P) of gates; and
the reconfigurable logic block is implemented with a second number (L) of gates; wherein:
the second number (L) is at least five times greater than the first number (P).

13. Multimedia interface, according to claim 12, wherein:
the at least one functional block is the CODECs; and
the CODECs is implemented with a third number (C) of gates; and
the second number (L) is at least six times greater than the third number (C).

14. Multimedia interface, according to claim 12, wherein:
the at least one functional block is the CODECs; and
the CODECs is implemented with a third number (C) of gates; and
the first number (P) is 2-4 times greater than the third number (C).

15. Signal processing interface, comprising:
an integrated circuit (IC) chip;
a block of reconfigurable logic incorporated on the IC chip; and
a RISC core incorporated on the IC chip separately from the reconfigurable logic ;
further comprising at least one functional block selected from the group consisting of:
audio and/or video CODECs for interfacing to external analog multimedia signals;
phase locked loop (PLL) circuitry to reduce skew within various blocks within the IC chip and to synchronize to off-chip clock circuitry;
a programmable, fast serial interface core;
a programmable CPU interface core;
a programmable memory interface (PMI) core; and
power-down circuitry, in combination with one or more of these additional cores .

16. Signal processing interface, according to claim 15, wherein:
the RISC core is non-reconfigurable .

21. An electronic system incorporating at least one integrated circuit (IC) chip , said IC chip comprising:
a block of reconfigurable logic incorporated on the IC chip; and
a multimedia processor block incorporated on the IC chip separately from the reconfigurable logic;
further comprising at least one functional block selected from the group consisting of:
audio and/or video CODECs for interfacing to external analog multimedia signals;
phase locked loop (PLL) circuitry to reduce skew within various blocks within the IC chip and to synchronize to off-chip clock circuitry;
a programmable, fast serial interface core;
a programmable CPU interface core;
a programmable memory interface (PMI) core; and
power-down circuitry, in combination with one or more of these additional cores .

22. An electronic system, according to claim 21, wherein the electronic system is selected from the group consisting of general-purpose computer, telecommunication device, network device, consumer device, receiver, recorder, display device, and vehicle.

23. Multimedia interface , according to claim 3, wherein:
the multimedia processor block is non-reconfigurable.

24. An electronic system, according to claim 21, wherein:
the multimedia processor block is non-reconfigurable.

26. Multimedia interface, according to claim 27, wherein:
the reconfigurable logic is a field programmable gate array (FPGA).

27. Multimedia interface, comprising:
an integrated circuit (IC) chip;
a block of reconfigurable logic incorporated on the IC chip;
a multimedia processor hard macro incorporated on the IC chip; and
further comprising at least one functional block selected from the group consisting of:
audio and/or video CODECs for interfacing to external analog multimedia signals;
phase locked loop (PLL) circuitry to reduce skew within various blocks within the IC chip and to synchronize to off-chip clock circuitry;
a programmable, fast serial interface core;
a programmable CPU interface core;
a programmable memory interface (PMI) core; and
power-down circuitry, in combination with one or more of these additional cores.

28. Multimedia interface, according to claim 3, wherein the multimedia processor block is incorporated as a hard macro.